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(54) MOS varactor, in particular for radio-frequency transceivers

(57) A varactor (30) has a gate region (6), a first and a second biasing region (5a, 5b) of N^+ type, embedded in a well (4), and a first and a second extraction region (15a, 15b) of P^+ type, forming a pair of PN junctions (16a, 16b) with the well (4). The PN junctions (16a, 16b) are inversely biased and extract charge accumulating in the well (4), below the gate region (6), when the gate region (6) is biased to a lower voltage (V_G) than a predetermined threshold value.

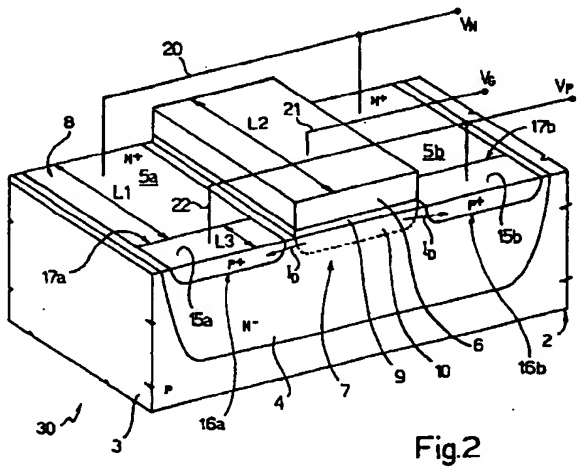

Fig.2

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Description

[0001] The present invention relates to a varactor, in particular for radio frequency transceivers.

[0002] As known, varactors are electronic devices having a variable capacity, selectable in particular through a biasing voltage, applied between a pair of terminals.

[0003] Varactors are used, for example, for tuning LC circuit radio-frequency transceivers. In fact, these circuits are adversely affected by production inaccuracies, and by the low quality factor of the passive components, and thus, in use, require adaptation of the actual reactance value, to adjust it to the planned values.

[0004] For this purpose a POS (Polysilicon-Oxide-Semiconductor) varactor has been recently proposed, described for example in the article "A ±30% Tuning Range Varactor Compatible with future Scaled Technologies", by R. Castello, P. Erratico, S. Manzini, F. Svelto, VLSI Symp. on Circuits, Dig. techn. papers, June 1998, pp. 34-35, and illustrated in figure 1. In detail, a varactor 1 is formed in a wafer 2, only partially shown for easy of representation, comprising a substrate 3, of P type, having a surface 8 and accommodating a well 4 of N^- type. In turn, the well 4 accommodates two biasing regions 5a and 5b, of N^+ type, spaced from one another, but electrically connected, as shown in the figure, by an electrical connection 20 and bias the well 4 to voltage V_N.

[0005] A gate region 6, made of polycrystalline silicon, extends above surface 8 of wafer 2, at an intermediate wafer portion 7 between biasing regions 5a and 5b, and is electrically isolated from the wafer portion 7 by a gate oxide region 9. The gate region 6 is biased to a voltage V_G, via an electrical connection line 21.

[0006] As apparent to those skilled in the art, the conductivity of the wafer portion 7 depends on the voltage difference $V_{VAR} = V_G - V_N$ existing between gate region 6 and well 4. In particular, when the gate region 6 is biased to a positive voltage V_G, in the wafer portion 7 charges (electrons) are accumulated and the capacity of the varactor 1 increases to a value CMAX, beyond which it remains constant, and can no longer be modulated. This capacity value CMAX, equivalent to the capacity of gate oxide layer 9, is reached for values of V_{VAR} slightly higher than 0 V (for example 0.3 - 0.4 V). If, on the other hand, voltage V_{VAR} is negative, in the wafer portion 7 a depletion region 10 is formed, the depth whereof increases along with the absolute value of inverse voltage V_{VAR}, thus causing the capacity of the varactor 3 to decrease down to a minimum value CMIN, when the inverse voltage V_{VAR} reaches a negative threshold value V_T (for example of approximately -1.6 V). In fact, below the threshold value, in the wafer portion 7, next to the surface 8 of the wafer 2, an inversion layer 11 is formed, comprising minority carriers (here gaps), thermally generated in the depletion region 10. The wafer portion 7 thus defines a capacity modulation region. For example, in a typical MOS process, CMAX is approximately equivalent to 500 nF/cm^2, and CMIN is approximately equivalent to 250 nF/cm^2.

[0007] However, the present production technology for integrated transceivers requires more extensive variability.

[0008] The object of the present invention is to provide a varactor, the capacity of which can be modified within a wider range than those obtained at present.

[0009] According to the present invention, a varactor is provided, as defined in claim 1.

[0010] For the understanding of the invention, an embodiment is now described, purely by way of non-limiting example, with reference to the attached drawings, in which:

- figure 1 shows a cross-section through a wafer, incorporating a varactor of a known type;
- figure 2 shows a perspective cross-section through a wafer, incorporating a varactor according to a first embodiment of the present invention;
- figure 3 shows a plan view of a wafer comprising a varactor, in a second embodiment of the present invention; and
- figure 4 shows a perspective cross-section through a wafer, incorporating a varactor according to a third embodiment of the present invention.

[0011] With reference to figure 2, in which parts equivalent to figure 1 are indicated with the same reference numbers, a varactor 30 is formed in a wafer 2 of semiconductor material, accommodating a well 4 of N^+ type. Similarly to figure 1, the well 4 comprises two biasing regions 5a and 5b, of N^+ type, extending parallel, spaced from one another, for a length L1. The two biasing regions 5a and 5b are also connected electrically via a first electrical connection line 20, and bias the well 4 to voltage V_N.

[0012] In figure 2, the gate region 6, again of polycrystalline silicon, extends parallel to the biasing regions 5a, 5b, above the wafer portion 7, and is insulated by the gate oxide region 9, for a length L2, greater than L1. The gate region 6 is biased to voltage V_G by a second electrical connection line 21.

[0013] In addition, as shown in figure 2, two charge extraction regions 15a and 15b, of P^+ type, extend in continuation of one of the ends of the biasing regions 5a and 5b, for a length L3, equal to the difference between L2 and L1, for example to about one hundredth of L1. For example, L2 may have a length of 10 µm, L3 may be the minimum lithographic dimension (for example 0.35 µm), and L2 is 9.65 µm.

[0014] Thus, the charge extraction regions 15a and 15b and the well 4 form a first pair of PN junctions 16a and 16b, and, the charge extraction regions 15a and 15b and the biasing regions 5a and 5b form a second pair of PN junctions 17a and 17b respectively. The charge extraction regions 15a and 15b are electrically connected to one another by a third electrical connec-

tion line 22 and are biased to voltage V_P

[0015] For example, the well 4 may have a doping level of 2-3x10^{17}at/cm^3; the biasing regions 5a and 5b and the charge extraction regions 15a and 15b may have a doping level of approximately 10^{20}at/cm^3, with ions imparting opposite types of conductivity.

[0016] The varactor 30 functions as follows.

[0017] Similarly to the varactor 3 of figure 1, the capacity of the varactor 30 is determined by voltage $V_{VAR} = V_G - V_N$ applied between the gate region 6 and the well 4. In addition, voltage V_P of the charge extraction regions 15a and 15b is lower than voltage V_N, such that the pairs of PN junctions 16a and 16b, 17a and 17b are always inversely biased when in use. For example, if the biasing regions 5a and 5b are connected to ground (V_N = 0 V),and V_G varies between +0.4 and -3 V, the voltage V_P is advantageously -3 V.

[0018] When voltage V_{VAR} is positive or negative, but is greater than threshold voltage V_T, the charge extraction regions 15a, 15b do not intervene, and the varactor 30 acts in a manner similar to that described with reference to the varactor 3 of figure 1.

[0019] When the voltage V_{VAR} reaches the threshold value V_T, the minority carriers (holes) thermally generated in the depletion region 10, accumulate near the gate oxide region 9, by virtue of the electrical field. However, since the extraction regions 15a and 15b are set to a lower voltage than the well 4, they attract the minority carriers (holes), thus creating a diffusion current I_D through the first pair of PN junctions 16a and 16b, inversely biased. Consequently, the minority carriers are removed from the depletion region 10, and the formation of an inversion layer below the gate oxide region 9 is prevented.

[0020] The phenomenon of thermal generation of carriers can be considered virtually stationary, compared with the frequency of the voltage signals typical of the applications commonly using varactors (of approximately hundreds or thousands of MHZ). The variations of the diffusion current I_D thus do not influence variations in the capacity of the varactor 30, which therefore are determined only by the depth of the depletion region 10, set by voltage V_{VAR}.

[0021] The described varactor has the following advantages. First, the values selectable for the capacity of the varactor 30 may vary more extensively than for conventional varactors. In fact, as previously stated, removal of minority carriers from the depletion region 10 prevents the formation of the inversion layer 11 (figure 1). Consequently, the capacity of the varactor 30 can assume lower values than the value reached when the inverse voltage V_{VAR} is V_T. For example, the capacity of the varactor 30 can vary between approximately 4.4 and 1.7 pF, when V_{VAR} varies between +0.4 and -3 V. In addition, in the voltage range comprised between the maximum voltage and the threshold voltage, junctions 16a, 16b are inversely biased (thus forming diodes in the off state), and thus do not modify the normal behaviour of the varactor.

[0022] In addition, the reduction of the minimum capacity CMIN, obtained by removing the minority carriers from the depletion region 10, improves the linearity of the varactor, thus eliminating the distortion effects occurring in known varactors, when voltage V_{VAR} approaches threshold voltage V_T.

[0023] The fact that the extraction regions 15a and 15b are integrated with the device constitutes a further advantage. In fact, these regions can be biased to inverse voltages compatible with the supply voltages provided to the circuitry interacting with the varactor 30 and do not require specific components for biasing.

[0024] Finally, it is apparent that many modifications and variants can be made to the varactor described and illustrated here, within the scope of the invention, as defined in the attached claims.

[0025] In particular, as illustrated in figure 3, not to scale for the sake of simplicity, the gate region, here indicated at 6', can comprise a plurality of fingers 30, electrically connected at a respective end by a connection region 31, such that, in practice, the gate region 6' is comb-shaped. The fingers 30 are arranged parallel to one another, each overlapping a respective capacity modulation portion. When seen from above, the fingers 30 alternate with zones 32, formed inside the well 4, and each comprise a biasing region 32a, of N^+ type, and an extraction region 32b, of P^+ type. All biasing regions 32a are biased to the same voltage V_N, as shown schematically by a connection line 20', and all the extraction regions 32b are biased to the same voltage V_P as shown schematically by a connection line 22'. In this case, the overall capacity of the varactor is equivalent to the sum of the capacities associated with each finger 30, since the fingers are in parallel to each other.

[0026] In addition, with reference to figure 4, intermediate zones 40 of N type, with a lower doping level than the biasing regions 5a, 5b, but higher than the well 4 (for example of approximately 10^{18}-10^{19}at/cm^3) can be formed respectively between the biasing region 5a and the respective extraction region 15a, and between the biasing region 5b, and the respective extraction region 15b. In this case, the length of the gate region 6 is given by the sun of the dimensions, in the same direction, of each of the biasing regions 5a, 5b of the respective intermediate zone 40, and of the respective extraction region 15a, 15b.

[0027] The intermediate zones 40 advantageously do not require corresponding masking steps, but can b formed simultaneously with regions belonging to the components of the circuit connected to the varactor 30 (typically the drain extension regions of NMOS transistors). Thereby, the capability of withstanding voltages is improved between each biasing region 5a, 5b, and the respective extraction region 15a, 15b.

[0028] Finally, the varactor 30 can be manufactured in dual form, in particular by forming inside a well of P type, biasing regions of P^+ type, and extraction regions

of N^+ type; in this case the voltages applied to the different regions have an opposite polarity to the described one.

Claims

1. A varactor, comprising a semiconductor material body (4), having a first conductivity type and a first doping level; at least one biasing region (5a; 32a), having said first conductivity type, a second doping level, higher than the first doping level, and embedded in said semiconductor material body (4), adjacent to a capacity modulation portion (7) of said semiconductor material (4) body; and a gate region (6; 6'), of conductive material, arranged above, and electrically insulated from, said semiconductor material body (4), at said capacity modulation portion (7), characterised by charge extraction means (15a, 15b; 32b) connected to said capacity modulation portions (7) of said semiconductor material body (4).

2. A varactor according to claim 1, characterised in that said charge extraction means comprises at least a first extraction region (15a; 32b), of a second conductivity type, arranged laterally to said capacity modulation portion (7).

3. A varactor according to claim 2, characterised in that it further comprises a second biasing region (5b), of said first conductivity type, spaced from said first biasing region (5a) by said capacity modulation portion (7), and a second extraction region (15b), of said second conductivity type, said first and second extraction regions (15a, 15b; 32b) being adjacent to a respective one of said first and second biasing regions (5a, 5b), on both sides of said capacity modulation portion (7).

4. A varactor according to claim 2 or claim 3, characterised in that said first biasing region (5a) and said first extraction region (15a) are aligned with one another, in a zone of said semiconductor material body (4), having substantially a same length as the length (L2) of said gate region (6).

5. A varactor according to claim 3 or claim 4, characterised in that said first and second extraction regions (15a, 15b; 32b) form a pair of PN junctions (16a, 16b), together with the respective one of said first and a second biasing region (5a, 5b).

6. A varactor according to claim 3 or claim 4, characterised by a voltage withstanding region (40) between said first and second extraction regions (15a, 15b), and the respective one of said first and second biasing regions (5a, 5b), said voltage withstanding region (40) having said first conductivity type and a third doping level comprised between said first and said second doping level.

7. A varactor according to any one of claims 3-6, characterised in that said first and second extraction regions (15a, 15b) are electrically connected to one another by an electrical connection line (22).

8. A varactor according to any one of the preceding claims, characterised in that said gate region (6') is comb-shaped, has a plurality of fingers (30) extending above a corresponding plurality of capacity modulation regions; and in that said semiconductor material body (4) comprises a plurality of zones (32) alternating with said capacity modulation regions; each said zone comprising a respective biasing region (32a) and a respective extraction region (32b), adjacent to one another.

9. A varactor according to claim 8, characterised in that said biasing regions (32a) are connected electrically to each other (20'), and in that said extraction regions (32b) are connected electrically to each other (22').

10. A varactor according to any one of claims 2-9, characterised in that said first conductivity type is N, and said second conductivity type is P.

11. A method for modulating the capacity in a varactor, comprising a semiconductor material body (4), of a first conductivity type and a first doping level; at least a first biasing region (5a; 32a), having said first conductivity type, a second doping level, higher than the first doping level, and embedded in said semiconductor material body (4) adjacent to a capacity modulation portion (7) of said semiconductor material body (4); and a gate region (6; 6'), of conductive material, arranged above, and electrically insulated from, said semiconductor material body (4), at said capacity modulation portion (7), wherein said semiconductor material body (4) is biased to a first potential (V_N), said gate region, (6; 6') is biased to a second potential (V_G) different from said first potential, and such as to form a depletion region (10) in said capacity modulation portion (7), characterised in that charge is extracted from said capacity modulation portion (7) through at least one charge extraction region (15a, 15b; 32b) biased to a third potential (V_P), thereby attracting minority carriers (11) generated in said depletion region (10).

12. A method according to claim 11, characterised in that said first conductivity type is N, in that said charge extraction region (15a) is arranged laterally to said capacity modulation portion (7), and has P type conductivity, in that said second potential (V_G)

is lower than said first potential (V_N), and said third potential (V_P) is lower than, or the same as said second potential (V_G).

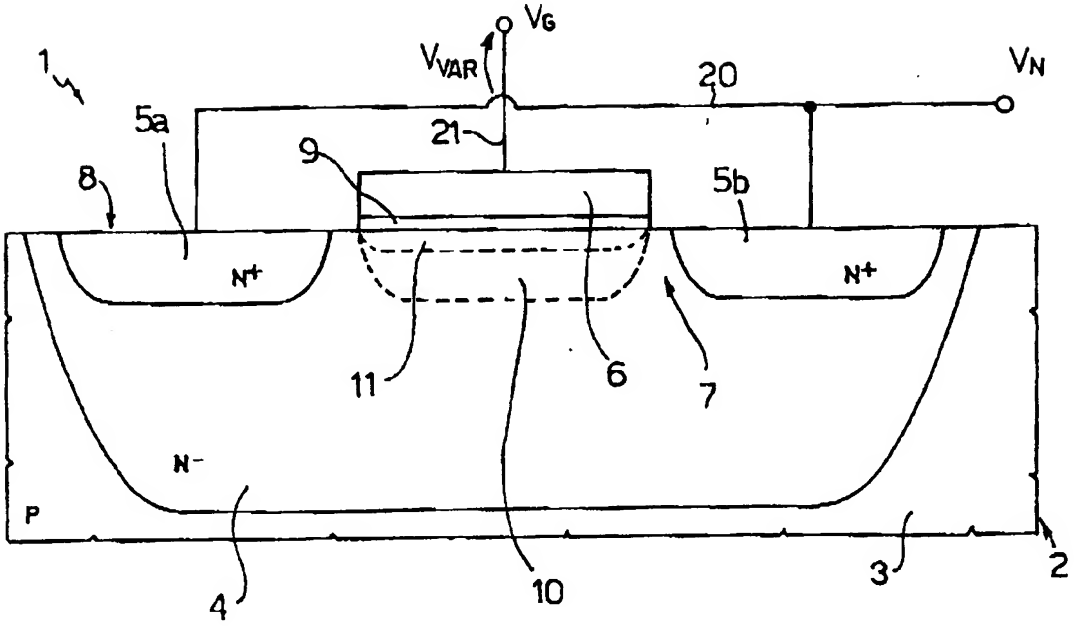

Fig.1

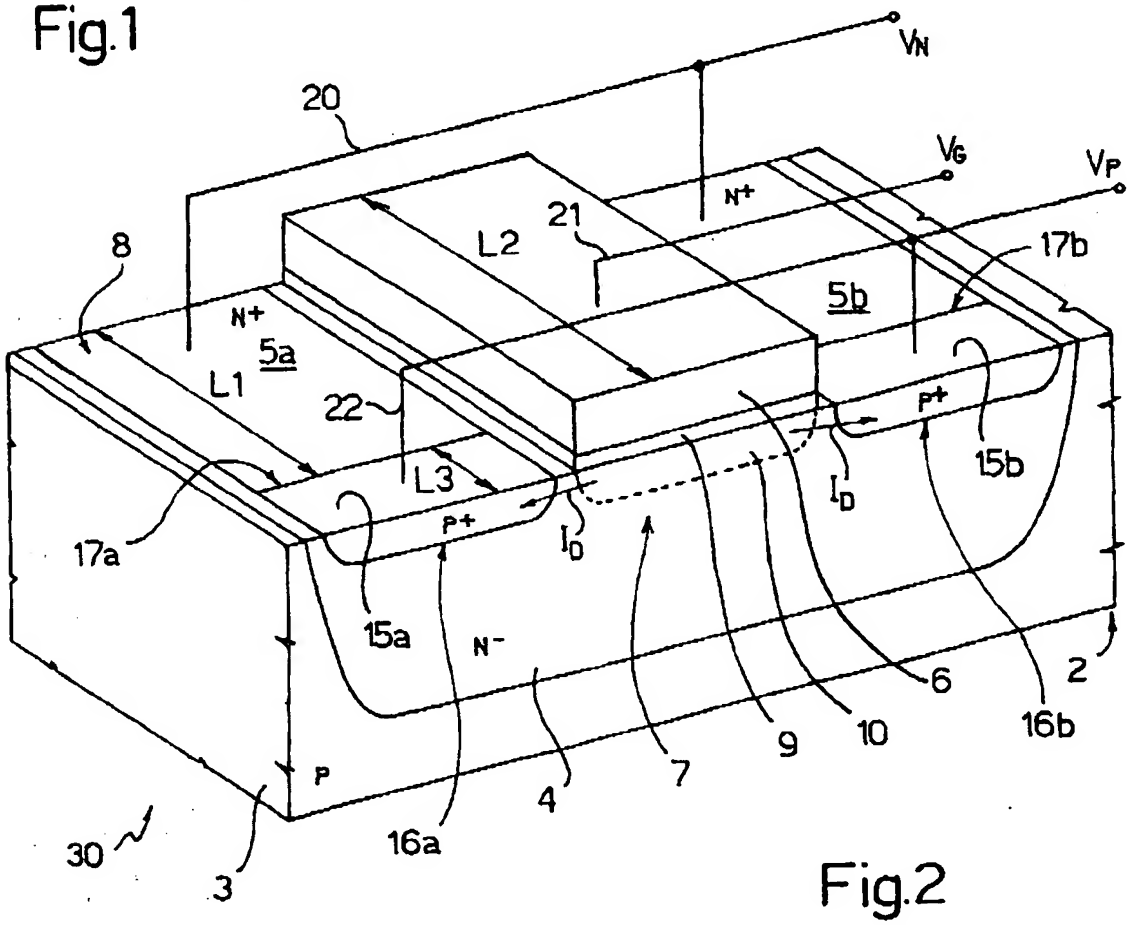

Fig.2

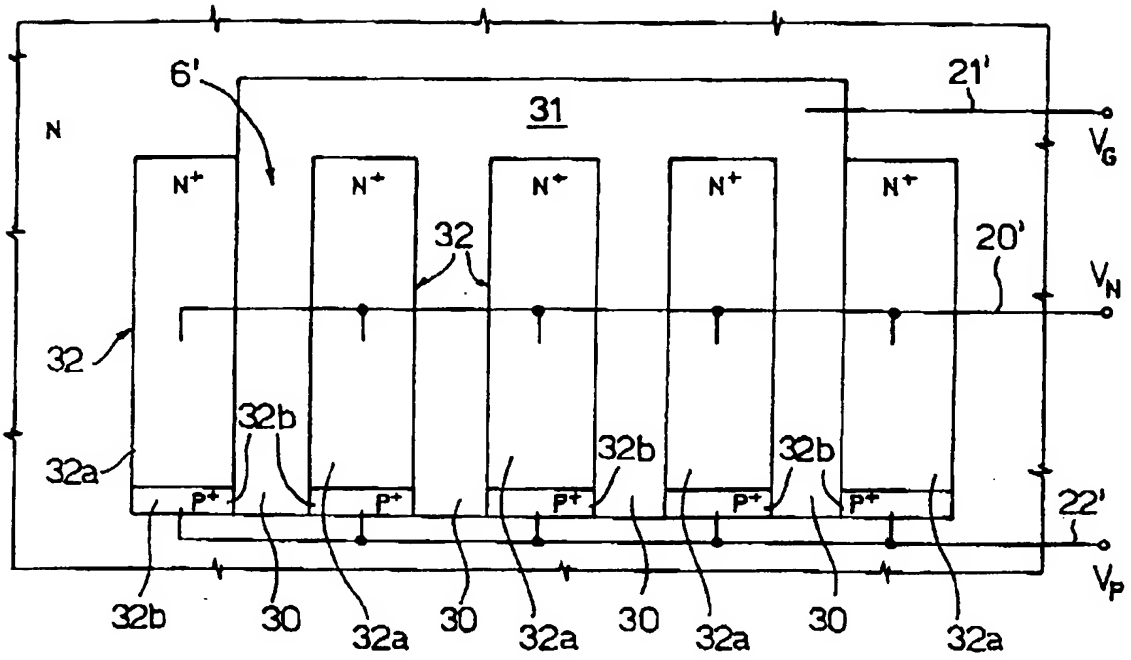

Fig.3

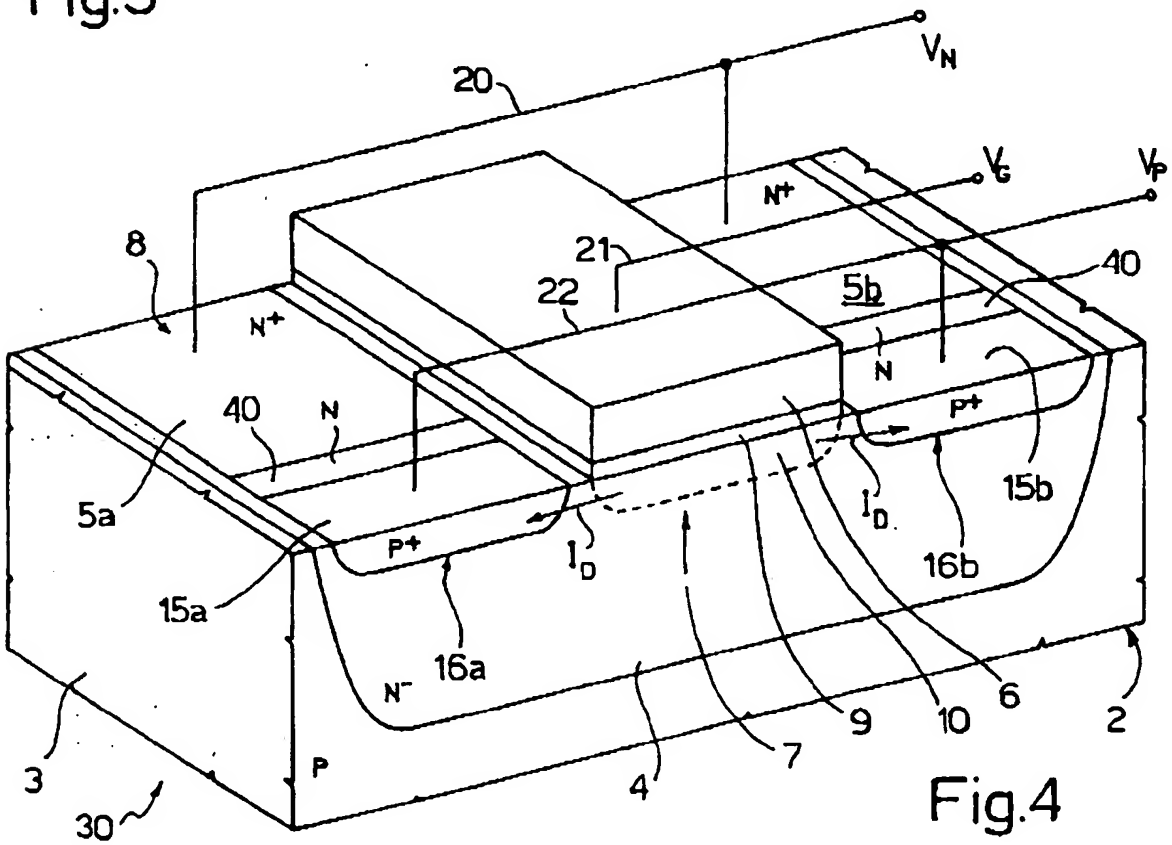

Fig.4

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EUROPEAN SEARCH REPORT

Application Number
EP 99 83 0044

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	2 June 1999	Polesello, P

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EUROPEAN SEARCH REPORT

Application Number
EP 99 83 0044

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